# VDHL Group 20 Testing Plan

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| HDB | RCB | Initial Release | Passed Pre-Synth | Passed Post-Synth | Comments |
| V0 | **V0** | 6/3 | N/A | N/A | * Initial commit of both blocks based on FSM logic and hand-out   + Includes draw dot * Not tested together * FSM state consolidation |
| V1 | **V1** | 13/3 | 14/3 | N/A | * Putting both blocks together   + Add clear screen * Test using sample commands |
| V1.1 | **V1.1** | 16/3 | 16/3 | 16/3 | * Debug corner cases   + Problems include: Sensitivity list, latch, octant table logic, xbias * Pass post synthesis * Pass custom corner case command test * Pass 100,000 random command test |
| “ | **V2** | 18/3 | 18/3 | 18/3 | * Increase speed of RCB block to have non-blocking flush * Pass both pre-post synthesis * Pass 100,000 random command test |